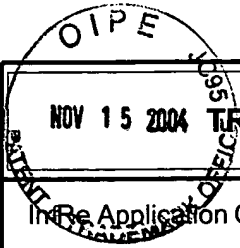
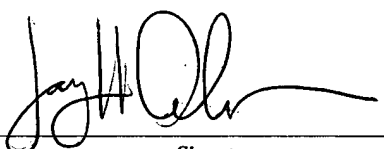


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				Docket No. FIS920030341US1	
In Re Application Of: <b>Victor Ku et al.</b>					
Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/707,759	01/09/2004		32074	2812	1758
Invention: <b>METHOD OF FORMING FET SILICIDE GATE STRUCTURES INCORPORATING INNER SPACERS</b>					
Address to: <b>Commissioner for Patents</b> <b>P.O. Box 1450</b> <b>Alexandria, VA 22313-1450</b>					
Transmitted herewith are:  8 sheets of formal drawing(s) for this application.  <input checked="" type="checkbox"/> Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).					
 _____ Signature			Dated: <i>12 November 2004</i>		
<b>Jay H. Anderson, Reg. No. 38,371</b> <b>IBM Corporation, IP Law</b> <b>2070 Route 52, Bldg. 300, Zip 482</b> <b>Hopewell Junction, New York 12533-6531</b> <b>845-894-3667</b>			I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on 11/12/2004 _____ (Date) <i>Nicole Barrese</i> 11-12-04 Signature of Person Mailing Correspondence <b>Nicole Barrese</b> Typed or Printed Name of Person Mailing Correspondence		